



# 128K x 24 Static RAM

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with  $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{CE3}$  and  $\overline{OE}$  options

## Functional Description<sup>[1]</sup>

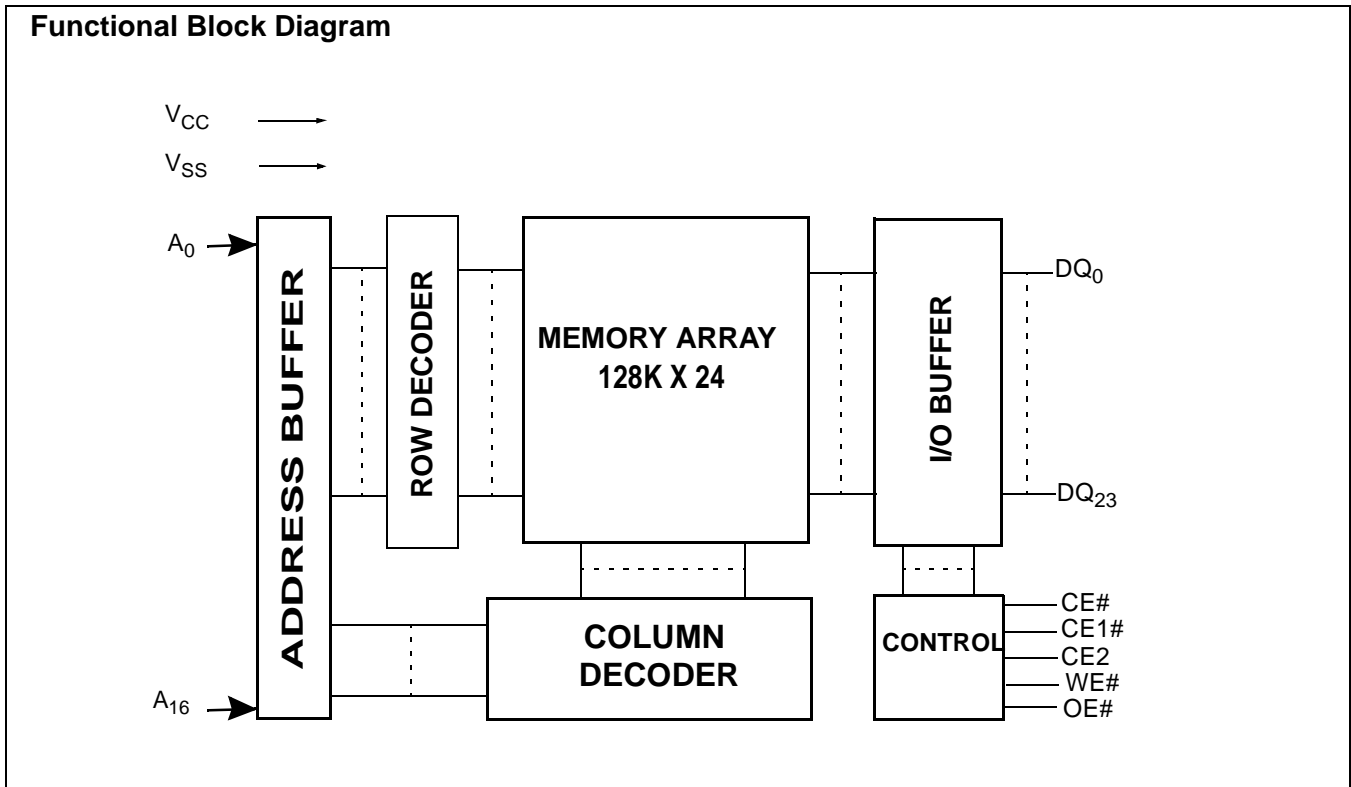
The CY7C1024AV33 is a high-performance CMOS static RAM organized as 131,072 words by 24 bits. Easy memory expansion is provided by an active LOW  $\overline{CE1}$ ,  $\overline{CE3}$ , active HIGH CE2, an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{CE3}$ ) active and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the 24 I/O pins ( $I/O_0$  through  $I/O_{23}$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{CE3}$ ) active and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 24 input/output pins ( $I/O_0$  through  $I/O_{23}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE1}$ ,  $\overline{CE3}$  LOW,  $\overline{CE2}$  HIGH, and  $\overline{WE}$  LOW).

The CY7C1024AV33 is available in a standard 119-ball BGA package and a 100-pin TQFP package.



## Selection Guide

	7C1024AV33-10	7C1024AV33-12	7C1024AV33-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	275	250	225
Maximum Standby Current (mA)	15	15	15

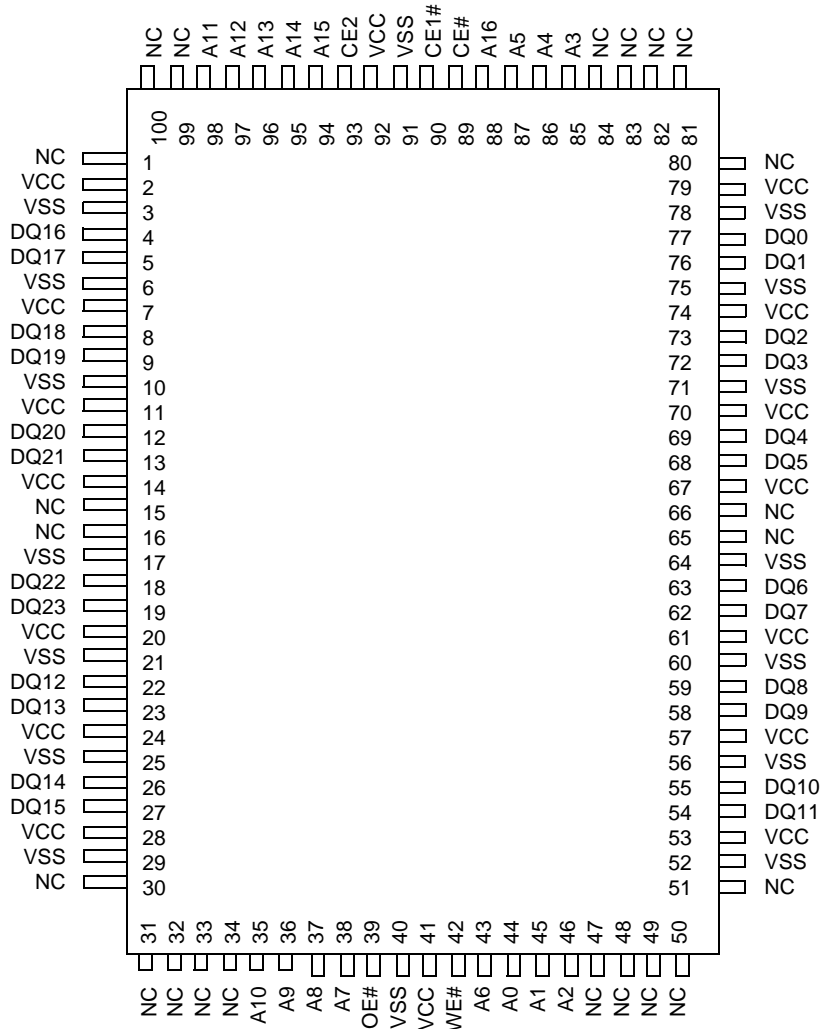
Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Pin Configurations**
**119 BGA  
Top View**

	1	2	3	4	5	6	7
<b>A</b>	NC	A	A	A	A	A	NC
<b>B</b>	NC	A	A	$\overline{\text{CE1}}$	A	A	NC
<b>C</b>	DQ	NC	CE2	NC	$\overline{\text{CE3}}$	NC	DQ
<b>D</b>	DQ	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	DQ
<b>E</b>	DQ	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	DQ
<b>F</b>	DQ	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	DQ
<b>G</b>	DQ	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	DQ
<b>H</b>	DQ	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	DQ
<b>J</b>	NC	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	NC
<b>K</b>	DQ	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	DQ
<b>L</b>	DQ	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	DQ
<b>M</b>	DQ	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	DQ
<b>N</b>	DQ	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	DQ
<b>P</b>	DQ	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	DQ
<b>R</b>	DQ	NC	NC	NC	NC	NC	DQ
<b>T</b>	NC	A	A	$\overline{\text{WE}}$	A	A	NC
<b>U</b>	NC	A	A	$\overline{\text{OE}}$	A	A	NC

**Pin Configurations** (continued)

**100-pin TQFP  
Top View**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[2]</sup>..... -0.5V to V<sub>CC</sub> + 0.5V

**Note:**

2. Minimum Voltage is = -2.0V for pulse durations of less than 20 ns.

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

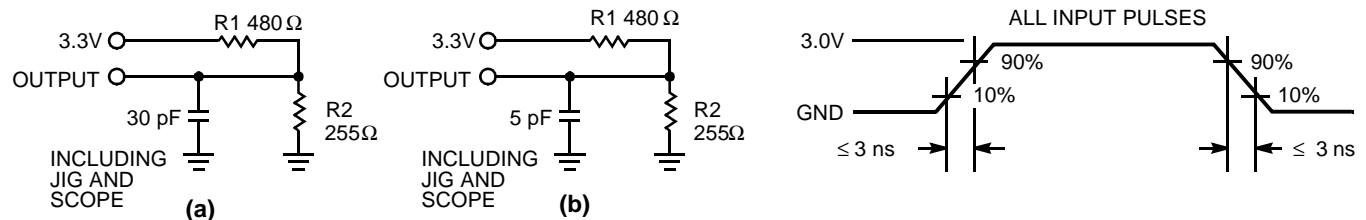
Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ±10%
Industrial	-40°C to +85°C	3.3V ±10%

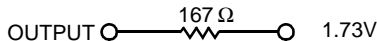
**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions <sup>[3]</sup>	1024AV33-10		1024AV33-12		1024AV33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-3	+3	-3	+3	-3	+3	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		275		250		225	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		60		60		60	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		15		15		15	mA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	10	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  


**Notes:**

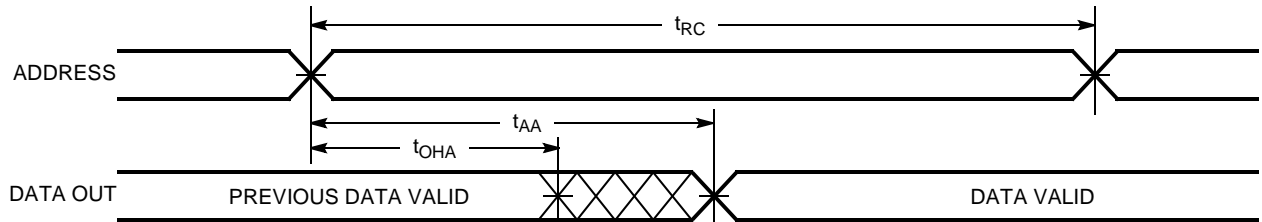
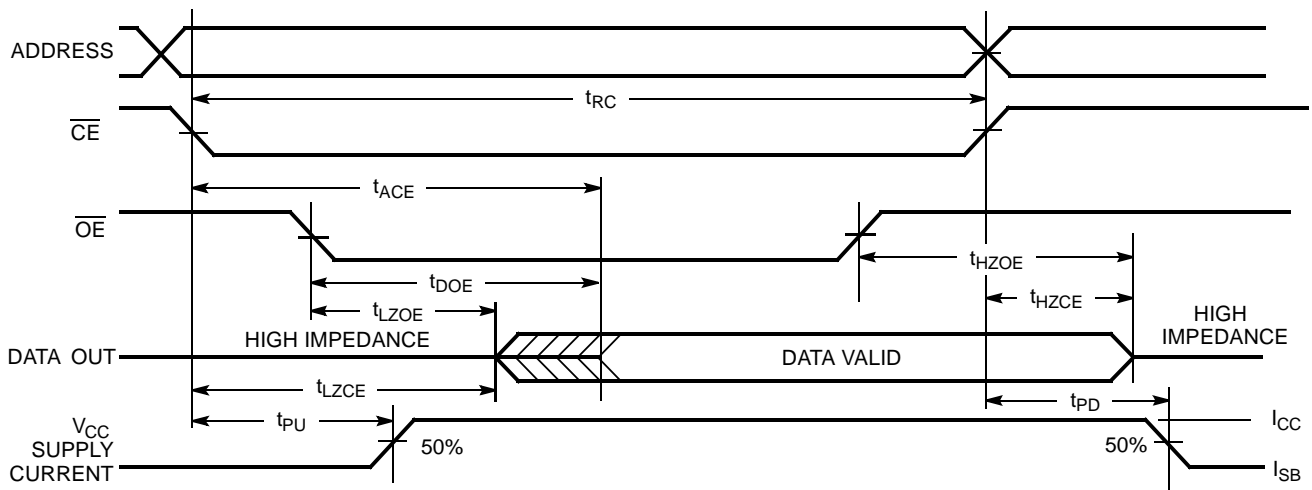
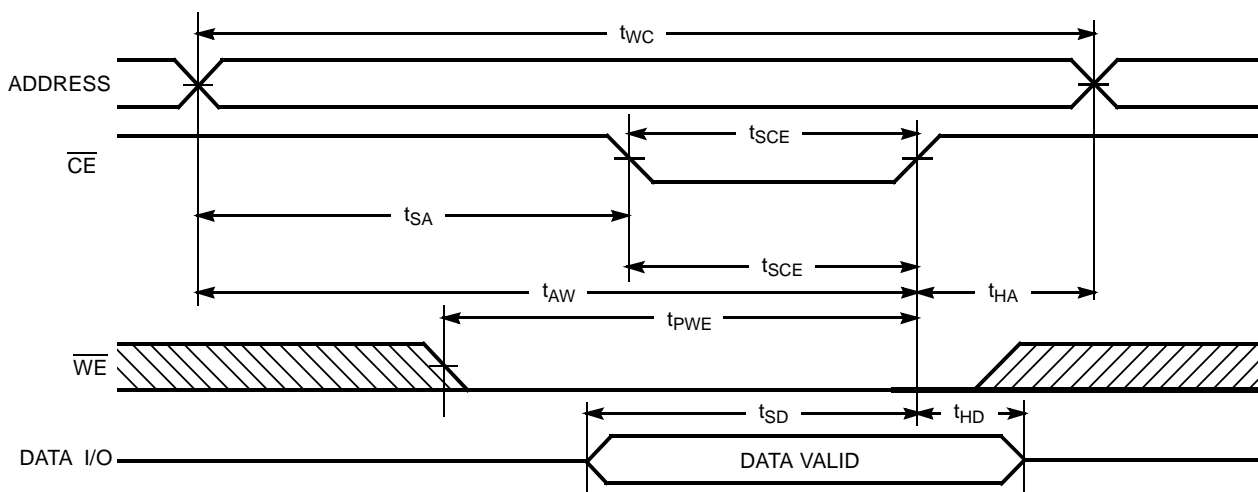
- CE is a combination of CE1, CE2, and CE3
- Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics<sup>[5]</sup> Over the Operating Range**

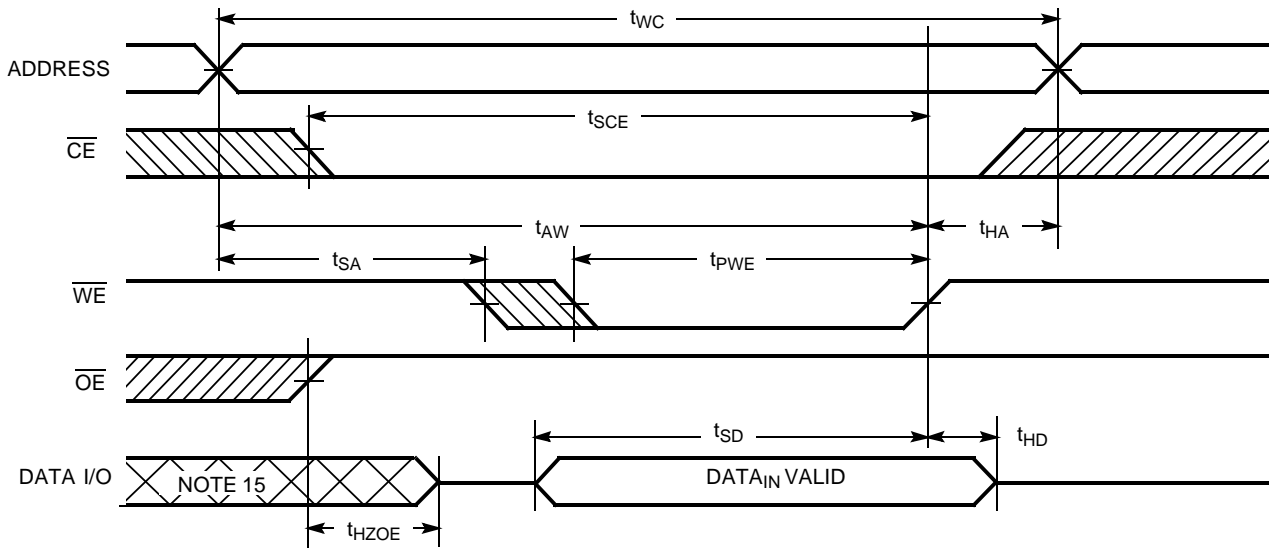
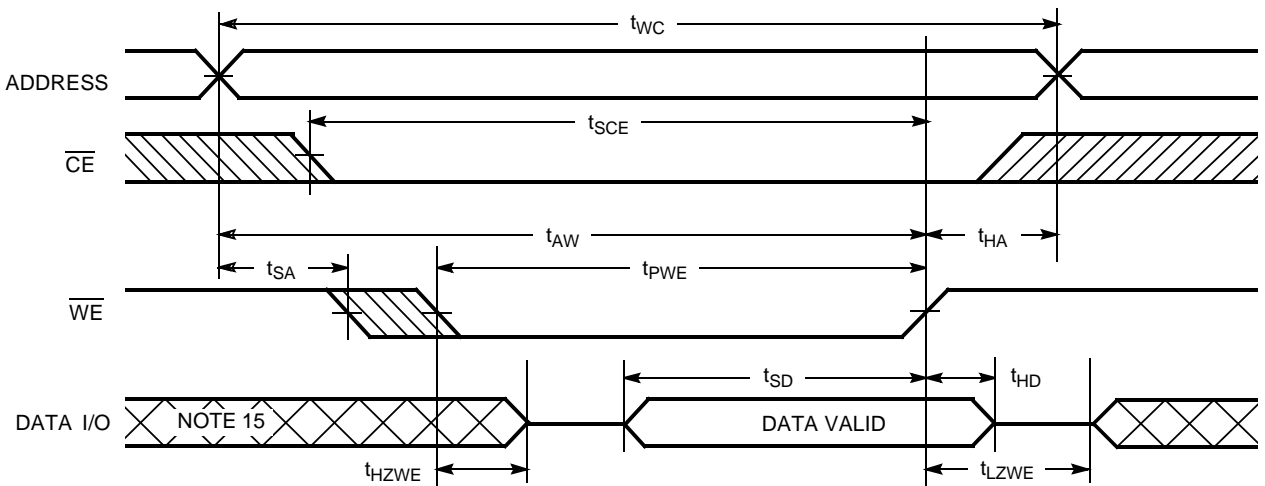
Parameter	Description <sup>[3]</sup>	7C1024AV33-10		7C1024AV33-12		7C1024AV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
$t_{RC}$	Read Cycle Time	10		12		15		ns
$t_{AA}$	Address to Data Valid		10		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}$ active to Data Valid		10		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		5		6		6	ns
$t_{LZCE}$	$\overline{CE}$ active to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ inactive to High Z <sup>[6, 7]</sup>		5		6		6	ns
$t_{PU}$	$\overline{CE}$ active to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ inactive to Power-Down		10		12		15	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>								
$t_{WC}$	Write Cycle Time	10		12		15		ns
$t_{SCE}$	$\overline{CE}$ active to Write End	8		9		9		ns
$t_{AW}$	Address Set-Up to Write End	7		8		8		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		8		8		ns
$t_{SD}$	Data Set-Up to Write End	5		6		6		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		5		6		6	ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Waveforms**
**Read Cycle No. 1**<sup>[10, 11]</sup>

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[3, 11, 12]</sup>

**Write Cycle No. 1 ( $\overline{CE}$  Controlled)**<sup>[3, 13, 14]</sup>

**Notes:**

10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>**

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[3, 14]</sup>**

**Note:**

15. During this period the I/Os are in the output state and input signals should not be applied.

**Truth Table**

CE1	CE2	CE3	OE	WE	I/O <sub>0</sub> -I/O <sub>23</sub>	Mode	Power
H	X	X	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
X	L	X	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
X	X	H	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	H	L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	H	L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	L	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

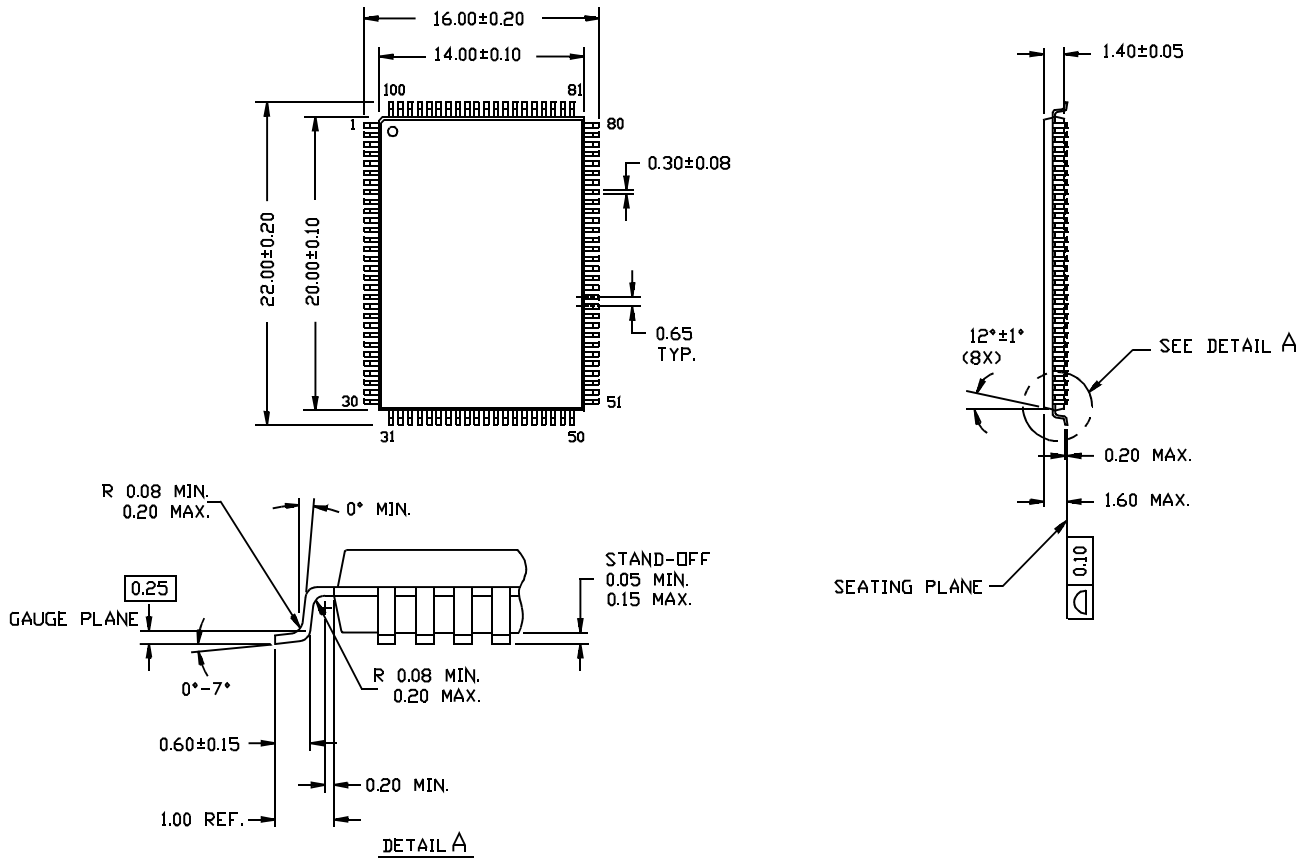
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1024AV33-10AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Commercial
	CY7C1024AV33-10BGC	BG119	119-Ball PBGA	
12	CY7C1024AV33-12AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Industrial
	CY7C1024AV33-12BGC	BG119	119-Ball PBGA	
	CY7C1024AV33-12BGI	BG119	119-Ball PBGA	
15	CY7C1024AV33-15AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Commercial
	CY7C1024AV33-15BGC	BG119	119-Ball PBGA	Industrial
	CY7C1024AV33-15BGI	BG119	119-Ball PBGA	



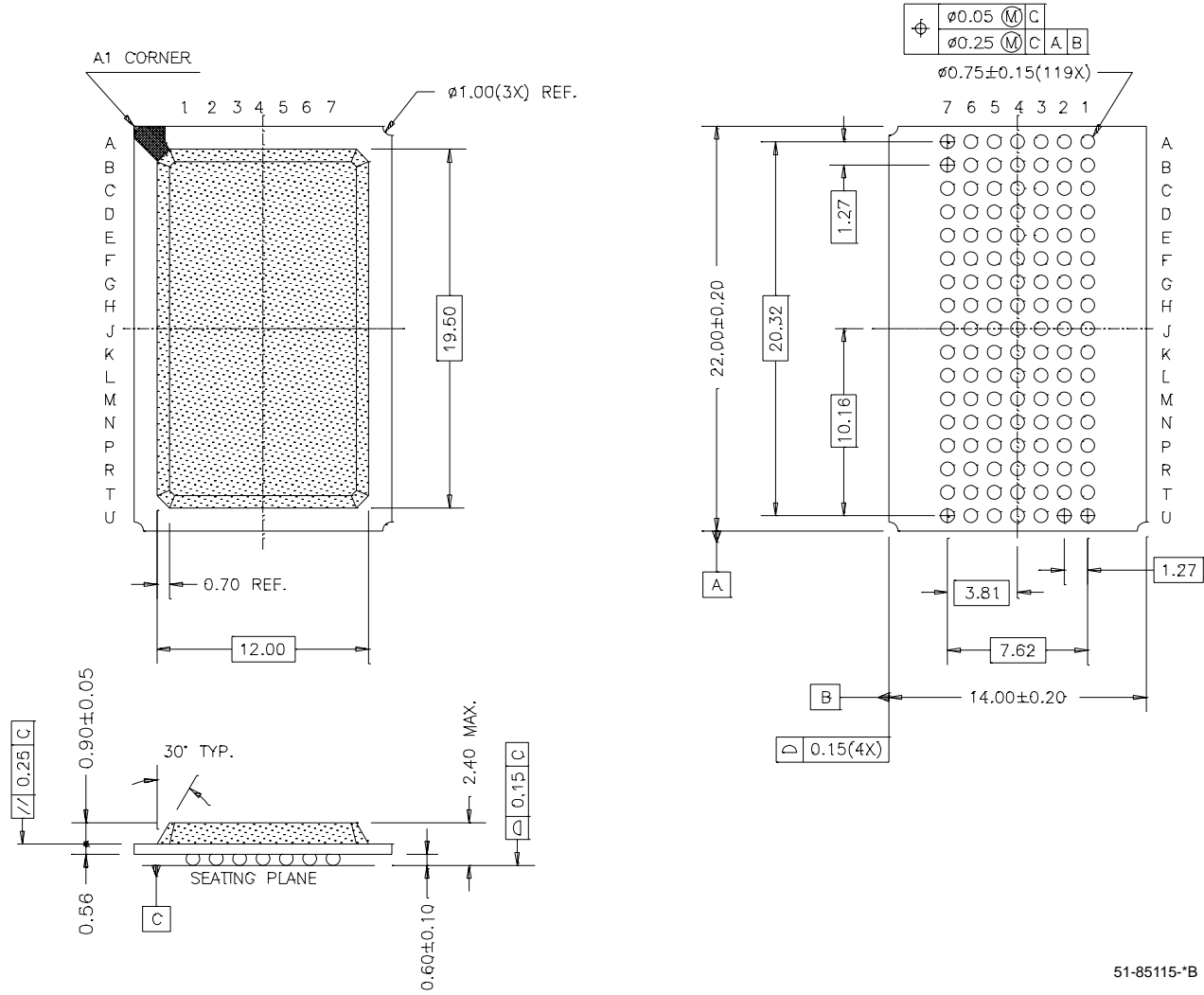
Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

DIMENSIONS ARE IN MILLIMETERS.



51-85050-A

**Package Diagrams (continued)**
**119-Lead PBGA (14 x 22 x 2.4 mm) BG119**


51-85115-B

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**Document History Page**

<b>Document Title: CY7C1024AV33 128K x 24 Static RAM</b>				
<b>Document Number: 38-05149</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109893	09/22/01	SZV	Change from Spec number: 38-00983 to 38-05149
*A	116473	09/16/02	CEA	Add applications foot note to data sheet, page 1.
*B	121472	11/14/02	DSG	Update package diagram 51-85115 (BG119) to rev. *B